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AMENDMENTS TO THE CLAIMS:

1-13. (Canceled)

14. (Currently amended) A[[n]] method of under color removal, the method comprising:

providing an initial color value as a minuend;

providing an under color value as a subtrahend wherein at least a most significant bit of said subtrahend is a sign bit; and

subtracting said subtrahend from said minuend to yield a carry-out signal and an output color result representing said initial color value net of said under color value;

limiting said result by:

logically ORing each bit of said result with the logical AND of said carry-out and said sign bit; and

logically ANDing each bit from said ORing step with the logical OR of said carry-out bit and said sign bit to yield an output bit.

15. (Previously presented) The method of Claim 14, said providing an initial color value comprising providing an 8-bit initial color value word.

16. (Previously presented) The method of Claim 14, said providing an initial color value comprising providing a word and said providing an under color value comprising providing a double word.

17. (Previously presented) The method of Claim 14, said providing an under color value comprising providing a 16-bit word.

18. (Previously presented) The method of Claim 14, said providing an under color value comprising providing a 16-bit word in which a most significant 8-bits have the same value.

19. (Previously presented) The method of Claim 14, said providing an under color value comprising providing a double word in which all of the bits in the most significant word have the same value.

20. (Previously presented) The method of Claim 14, said providing an initial color value comprising providing an initial color value in unsigned binary format.

21. (Previously presented) The method of Claim 14, said providing an under color value

comprising providing an initial color value in two's complement format.

22. (Currently amended) A circuit comprising:

a[[n]] processing unit receiving a minuend and a subtrahend and outputting a result equal to said minuend minus said subtrahend and a carry-out bit;

at least one first AND gate for logically ANDing said carry-out bit and a sign bit of said subtrahend;

at least one first OR gate for logically ORing said carry-out bit and a sign bit of said subtrahend;

at least one second OR gate for logically ORing each bit of said result with an output of said first AND gate;

at least one second AND gate for logically ANDing each output of said at least one second OR gate with an output of said first OR gate.

23. (Previously presented) The circuit of Claim 22, wherein said processing unit receives said minuend as an 8-bit binary word.

24. (Previously presented) The circuit of Claim 22, wherein said processing unit receives said subtrahend as an 8-bit two's complement word.

25. (Previously presented) The circuit of Claim 22, wherein said processing unit receives said subtrahend as a 16-bit two's complement word wherein a most significant 8 bits of said subtrahend are equal to a sign bit.